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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,881	09/28/2005	Stefan Marco Koch	CH 020024	8855
65913	7590	05/14/2008	EXAMINER	
NXP, B.V.			GIROUX, GEORGE	
NXP INTELLECTUAL PROPERTY DEPARTMENT				
M/S41-SJ			ART UNIT	PAPER NUMBER
1109 MCKAY DRIVE				2183
SAN JOSE, CA 95131				
			NOTIFICATION DATE	DELIVERY MODE
			05/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/521,881	KOCH ET AL.	
	Examiner	Art Unit	
	George D. Giroux	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 09 April 2008.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7, 9 and 10 is/are pending in the application.
 4a) Of the above claim(s) 8,11 and 12 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7, 9 and 10 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed 9 April 2008, in response to the Office Action mailed 10 January 2008. The applicant's remarks and amendments to the claims and specification were considered, with the results that follow.
2. Claims 8, 11 and 12 have been cancelled, while claims 1-7, 9 and 10 remain pending in this application.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9 April 2008 has been entered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koch (US 2002/0055979) in view of Tang (US 6,775,717).

As per claim 1, Koch teaches a first processor bus as **[a first processor bus 40 (paragraph 0050 and figure 4)]**, a first processor connected to the first processor bus as **[a first processor P1 is connected to a processor bus 40 (paragraph 0050 and figure 4)]**, a first direct memory access unit with an external direct memory access channel, and connected to the first processor bus as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4)]**, a first programmable unit--programmable by the first processor being connectable, via the first external direct memory access channel, to the first direct memory access unit as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045)]**, a first shareable unit being connectable to the first processor bus as **[shareable unit 43 connected to processor bus 40 (figure 4)]**, a second processor bus as **[the second processor bus 50 (paragraph 0050 and figure 4)]**, a second processor connected to the second processor bus as **[a second processor P2 that also has a processor bus 50 (paragraph 0050 and figure 4)]**, a second direct memory access unit with an external direct memory access channel, and connected to the second processor bus as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4)]**, a second programmable unit--programmable by the second processor--being connectable, via the

second external direct memory access channel, to the second direct memory access unit as **[access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045)]** and a second shareable unit being connectable to the second processor bus as **[shareable unit 53 connected to the processor bus 50 (figure 4)], wherein the first programmable unit and the second programmable unit each comprise a processor interface, and a direct access unit core as [the access unit comprises a processor interface, a direct access unit (DAU), and external DMA channel interface (paragraph 0045 and figure 3)]** and wherein a first bi-directional communication channel is established between the first shareable unit and the second processor, and a second bi-directional communication channel is established between the second shareable unit and the first processor as **[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051)].**

Koch does not explicitly teach wherein the first programmable unit and the second programmable unit each comprise two external direct memory access channel interfaces, however.

Tang teaches wherein the first programmable unit and the second programmable unit each comprise two external direct memory access channel interfaces as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA**

channel interface providing a DMA channel request for a next DMA transfer (column 2, lines 42-55)].

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch.

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)].**

As per claim 2, Koch teaches wherein the first and/or second bi-directional channels are half-duplex channels or full-duplex channels as **[the access unit 48 provides a half-duplex channel to and from the processor bus 40 and the DMA unit 54 (paragraph 0055)].**

As per claim 3, Koch teaches wherein both processors are similar from an architectural point of view as **[processors P1 and P2 are similar from an architectural point of view (claim 2)].**

As per claim 4, Koch teaches wherein the processors are implementations of the same type of processor design as **[processors P1 and P2 are implementations of the same type of processor design (claim 3)].**

As per claim 5, Koch teaches wherein the processors are implementations of different types of processor design as **[processors P1 and P2 are implementations of different types of processor design (claim 4)].**

As per claim 6, Koch teaches wherein the shareable unit is a memory, a peripheral, an interface, an input device or an output device as **[examples of shareable units are: volatile memory, non-volatile memory, peripherals, interfaces, input devices, output devices, and so forth (paragraph 0044)].**

As per claim 7, Koch teaches wherein one of the two processors is a CPU, a microprocessor, a DSP, a system controller, a co-processor or an auxiliary processor as **[the processors described can be any of the following: a CPU, a microprocessor, a DSP, a system controller, a co-processor, an auxiliary processor, and so forth (paragraph 0043)].**

As per claim 9, Koch teaches wherein the processor interface has a programming link for either connecting to a corresponding processor bus or for connecting to a corresponding processor as **[the access unit has a data link 33 and a**

control link 34 for connection to the processor bus (paragraph 0045 and figure 3)].

As per claim 10, Koch teaches wherein the first and second bi-directional communication channels transfer data and/or control information to and from the first and second shareable units via the communication channels as **[each communication channel is employed for transferring data and/or control information to and from the shareable units (claim 11)].**

Response to Arguments

6. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Tang (US 6,775,717) teaches the use of two external DMA channel interfaces for readying multiple DMA channel requests within the same unit simultaneously.

Conclusion

7. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**: claims 8, 11 and 12 have been cancelled; claims 1-7, 9 and 10 are rejected.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Nair (US 5890013) - teaches an inter-processor communication system in which each processor has private data and program busses, and these busses are connected to shared memory banks which can be switched between processors.

b. Sunahara (US 5093780) - teaches an inter-processor communication system where each processor writes communication information to a shared memory, and a data link controller transfers data to a memory attached to a second processor automatically.

9. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

10. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Giroux whose telephone number is (571)272-

9769. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/George D Giroux/
Examiner, Art Unit 2183